9.3 Panel-Sized TFT-LCD Column Driver

O. Ishibashi, M. Iriguchi, K. Kimura, J. Ishii, D. Sasaki, H. Imai, H. Tsuchi, H. Hayama

NEC, Sagamihara, Japan

Panel-sized drivers (PSDs) are LSIs whose length is nearly equal to the width or height of an LCD, and they have long narrow shapes and identical outputs for scan/column lines. Conventional modules need PCBs for signal distribution and power supply, and tape carrier packages (TCPs) in many cases, as shown in Fig. 9.3.1. On the other hand, PSD modules only need drivers assembled directly on the LCD panel and do not need any PCBs or TCPs because the PSD has all the functions of the drivers, TCPs, and PCB. Furthermore, PSDs are fabricated with large rectangular glass substrates using System-On-Glass (SOG) technology (LTPS CMOS TFT) and thus are fabricated at a reasonable cost. In addition, assembly reliability is better than that of conventional modules because both PSDs and LCDs are fabricated on glass substrates that have the identical thermal expansion coefficient. We have fabricated a prototype panel-sized scan driver (PSSD) for a 12in. XGA TFT-LCD [1] and have successfully demonstrated assembled PSSDs [2]. In this paper, we report a prototype 6b color panel-sized column driver (PSCD) for 15in. XGA amorphous silicon (a-Si) TFT-LCDs. Two types of PSCDs have been fabricated. One is the 3072-output full-sized PSCD whose length is nearly equal to the width of a 15in. XGA TFT-LCD, and the other is the 1536-output half-sized PSCD whose length is nearly half of the full-sized PSCD. Considering the yield of PSCDs, half-sized PSCDs have been fabricated as a result.

A problem of PSCDs is that the operation speed of SOG-TFTs is slower than that of bulk silicon MOS transistors (MOSTs), and the uniformity of device characteristics of SOG-TFTs is worse than that of bulk MOSTs. Furthermore, it is necessary for data- and control-signals that are entered into PSCDs to be transmitted through conductors whose lengths are approximately 300mm, which corresponds to the width of 15in. LCDs.

We have confirmed that circuits composed of widely used SOG-TFTs have operated at a maximum speed of approximately 20MHz. Therefore, we decided to set the operating clock frequency of full-sized PSCDs to 16.25MHz, which corresponds to 1/4 of that of the 65MHz dot clock when the frame rate is 60 frames/s and the display resolution is XGA. Consequently, the internal data of PSCDs is transmitted in a 72b-wide data field, which is quadruple that of 6b RGB data. Similarly, the input data interfaces on PSCDs are 72b parallel data bus interfaces. The operating clock frequency in half-sized PSCDs is 8.125MHz because the data transmission during a horizontal period in half-sized PSCDs is 1/2 of that of full-sized PSCDs.

As mentioned above, signals in PSCDs are transmitted through conductors that are approximately 300mm long, so we were concerned about signal degradation and latency caused by conductor resistances and floating capacitances. Therefore, 40μm-wide and 17μm-thick copper-plated low-resistance conductors were adopted for a clock (CLK) signal line that drives 256b shift registers and for a latch pulse (LP) signal line for load latches. CLK and LP are transmitted through a 300mm-long conductor with a buffer. Consequently, edge rates (from 10% to 90%) of the transmitted CLK and LP are less than 16ns and their latencies are less than 1ns, which are sufficient to drive all shift registers and all load latches at the desired speed simultaneously. In addition, copper-plated conductors were also used for power supply lines to reduce voltage drop. Conventional column drivers often use a data bus for the data signal transmission, as shown in Figure 9.3.2. However, it is not realistic for a data bus to use copper-plated conductors. The 72b data bus is 7.2mm wide because copper-plated conductors on SOG devices, which can be made using current technology, have dimensions where the narrowest width is 40μm and the narrowest space is 60μm. Therefore, the data transfer system using 72×256-bit shift registers was used in the first prototype PSCDs, as shown in Fig. 9.3.2.

A block diagram of the prototype full-sized PSCDs is shown in Fig. 9.3.3. The output buffer consists of a positive-polarity driving amplifier (P-AMP) and a negative-polarity driving amplifier (N-AMP), whose outputs are alternated by an output switch per horizontal period. Large offset voltages are generated at the P- and N-AMPs in many cases. As mentioned above, because the uniformity of the characteristics of SOG-TFTs is worse than that of bulk silicon MOSTs, SOG-TFT amplifiers have larger offset voltages than those of bulk MOST amplifiers. We require that the output voltage deviation have 6b DAC precision (output deviation $< |20mV|$), so the offset voltage needs to be as small as possible. Therefore, an offset cancellation scheme was adopted for the voltage follower amplifier, as shown in Fig. 9.3.4. In the first 10μs during a 20μs horizontal period, after the output voltage is stabilized using fast driving, an offset voltage (ΔV) with a value between the input voltage (V_{IN}) and the output voltage (V1) is generated. An offset cancel capacitance (C_{OC}) holds ΔV. In the next 10μs the voltage follower amplifier cancels the offset voltage in the output voltage (V_{OUT}) using the ΔV that was held by C_{OC}. To confirm grayscale voltage characteristics of PSCD output, we evaluated transient waveforms of a PSCD output while input data codes were increased one step per 20μs horizontal period, and the measured results are shown in Fig. 9.3.4. Offset voltages before and after the cancellation for 190 outputs (P-AMP) are also shown in Fig. 9.3.4. We have confirmed that the PSCDs were able to output the desired voltages according to the input data. Furthermore, as shown in the enlarged inset in Fig. 9.3.4, the PSCDs were able to cancel the offset voltage within the later 10μs. Offset voltages of P-AMP during the offset detection period were in a range from -400mV to 400mV, and those of N-AMP were in a range from -600mV to 600mV. As a result of offset cancellation, the PSCD achieved an output deviation of $|20mV|$ in one 20μs horizontal period and substantially reduced offset voltage.

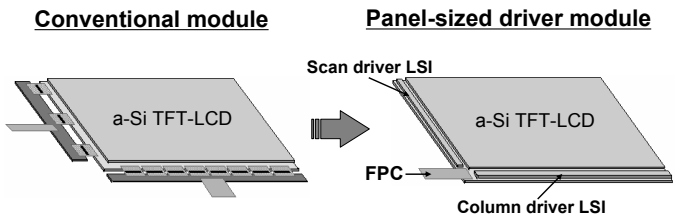
Specifications and a chip micrograph of a PSCD are shown in Figs. 9.3.5 and 9.3.6, respectively. The pads on PSCDs are copper-plated bumps and are aligned at intervals of 96μm in a zigzag. Finally, PSCDs were assembled using an anisotropic conductive film, and display operation of 15in. XGA TFT-LCDs has successfully been demonstrated. The design rule of TFTs in analog circuits is 4μm, and that of in logic circuits is 2μm. Full-sized PSCDs and half-sized PSCDs are composed of approximately 2 and 1 million TFTs, respectively. If TFTs with more uniform characteristics are used, the circuit area and consumption current can further be reduced.

References:

[1] D. Sasaki et al., "A Panel-Sized TFT-LCD Scan Driver," *ISSCC Dig. Tech. Papers*, pp. 556-557, Feb., 2005.

[2] S. Noda et al., "Flip Chip Assembly of Panel-Sized TFT-LCD Scan Drivers with Electroless-Planed Bumps using Anisotropic Conductive Films," *SID Dig.*, pp. 1788-1791, May, 2005.

 1-4244-0079-1/06/$20.00



Problems
(1) Bulky connection PCBs
(2) Expensive tape carrier package (TCP)
- comparable price with driver LSIs
(3) Over ten parts for assembly

New modules need
(1) No PCBs,
(2) No TCPs, and
(3) Only three parts for assembly.

Figure 9.3.1: Panel-sized driver concept.

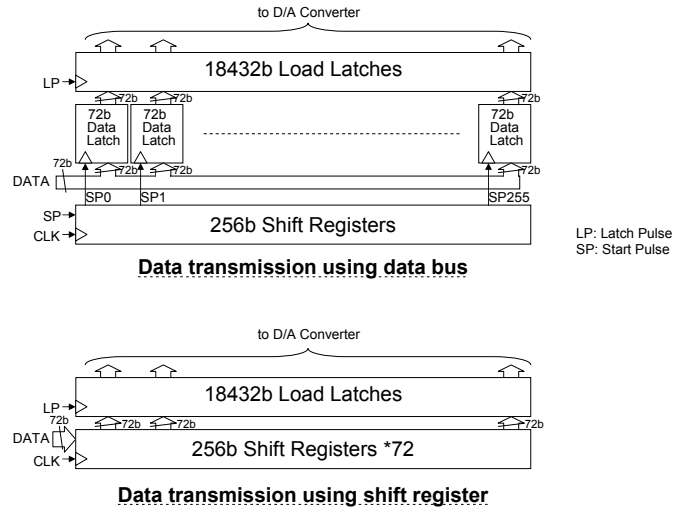


Figure 9.3.2: Data transmission methods.

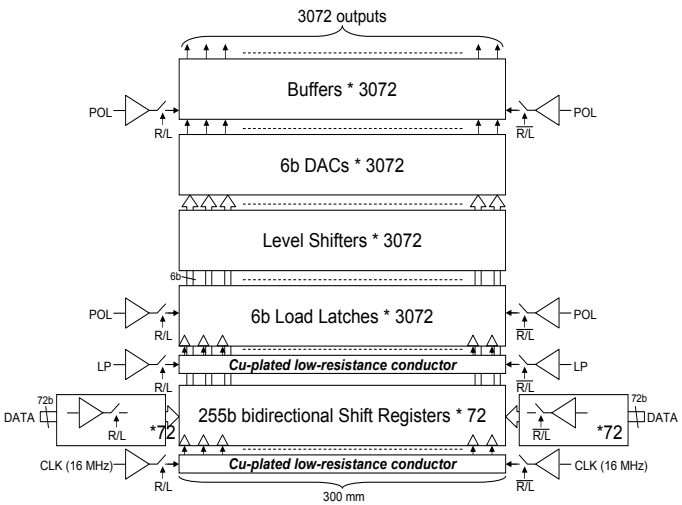


Figure 9.3.3: Block diagram of panel-sized column driver.

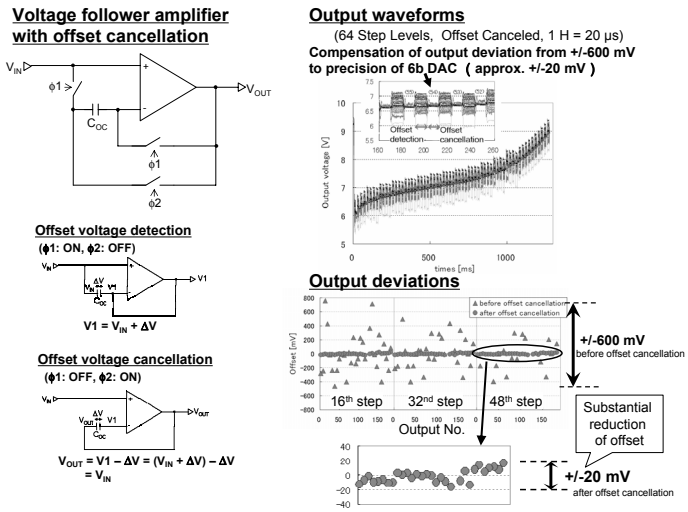


Figure 9.3.4: Offset cancellation amplifier and measurement result.

Application	**15-inch XGA a-Si TFT-LCDs**
Inputs	**6b RGB data * 4 (0V/3.3 V CMOS)**
Outputs	**64 step levels (deviation: < +/-30 mV)**
Output pins	**3072 (Full-sized) 1536 (Half-sized)**
Output pin pitch	**96 µm (Zigzag alignment)**
Power supply voltage	**Analog 10 V Logic 5 V**
Output voltage	**Negative polarity: 4.1 V~0.7 V Positive polarity: 6.0 V~9.4 V**
Driver size	**298 mm * 7.92 mm (Full-sized) 151 mm * 7.92 mm (Half-sized)**
Process	**LTPS TFT CMOS Analog 4 µm Logic 2 µm**
Number of TFTs	**approx. 2 million (Full-sized) approx. 1 million (Half-sized)**
Operating frequency	**16.25 MHz (Full-sized) 8.125 MHz (Half-sized)**
Functions	**Bidirectional data transmission Output voltage polarity inverting Line inverting Dot inverting**
Conductor	**Low-resistance conductor with copper plating**

Figure 9.3.5: Specifications.

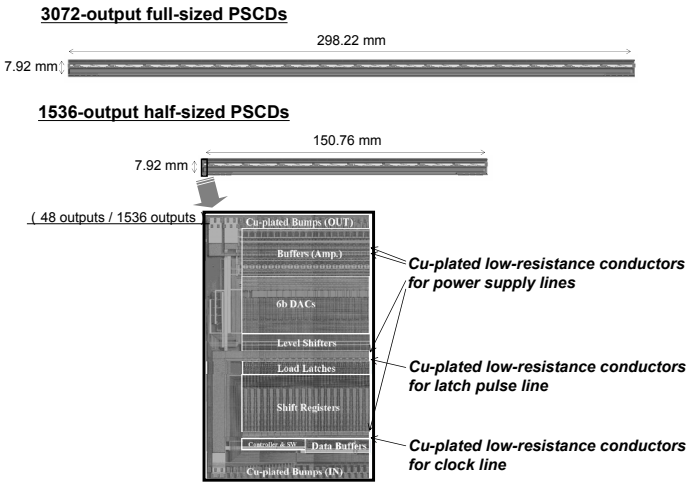


Figure 9.3.6: Chip micrograph.